CY62146E MoBL®

4-Mbit (256 K × 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) Type II package

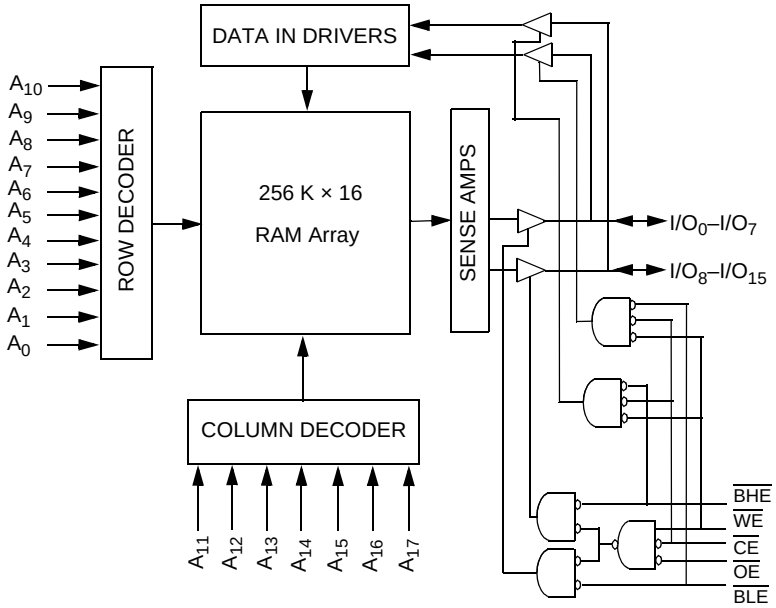
Functional Description

The CY62146E is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH) or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See Truth Table on page 11 for a complete description of read and write modes.

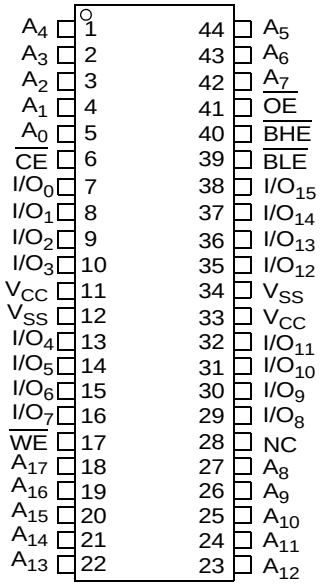
Logic Block Diagram



Contents

Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View) [1]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62146ELL	Industrial / Automotive-A	4.5	5.0	5.5	45	2	2.5	15	20	1	7

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to 6.0 V

DC voltage applied to outputs in high Z state [3, 4] .....–0.5 V to 6.0 V

DC input voltage [3, 4] .....–0.5 V to 6.0 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .....>2001 V

Latch-up current .....>200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62146ELL	Industrial / Automotive-A	–40 °C to +85 °C	4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Industrial/Automotive-A)			Unit
				Min	Typ [6]	Max	
V_{OH}	Output high voltage	I_{OH} = –1.0 mA		2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA		–	–	0.4	V
V_{IH}	Input high voltage	4.5 ≤ V_{CC} ≤ 5.5		2.2	–	V_{CC} + 0.5	V
V_{IL}	Input low voltage	4.5 ≤ V_{CC} ≤ 5.5		–0.5	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = 1/t_{RC}	V_{CC} = V_{CCmax}	–	15	20	mA
		f = 1 MHz	I_{OUT} = 0 mA, CMOS levels	–	2	2.5	
I_{SB2} [7]	Automatic CE power down current – CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$		–	1	7	µA

Notes

3. V_{IL}(min) = –2.0 V for pulse durations less than 20 ns for I < 30 mA.
4. V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. Full Device AC operation assumes a minimum of 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs are left floating.

Capacitance

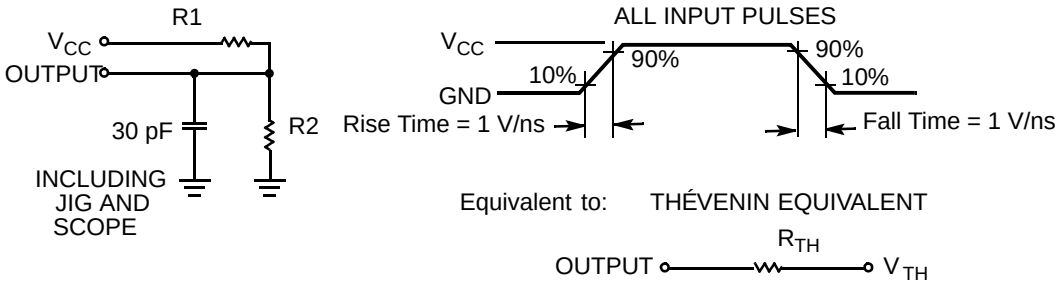
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two layer printed circuit board	77	°C/W
Θ_{JC}	Thermal resistance (junction to case)		13	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V

Note
8. Tested initially after any design or process changes that may affect these parameters.

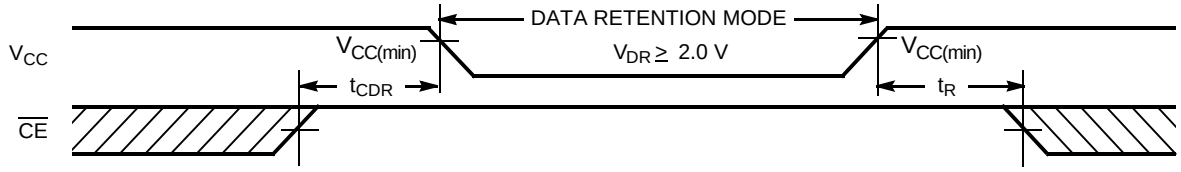
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention		2	–	–	V
I_{CCDR} [10]	Data retention current	V_{CC} = 2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	1	7	µA
t_{CDR} [11]	Chip deselect to data retention time		0	–	–	ns
t_R [12]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs are left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [13, 14]	Description	45 ns (Industrial / Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [15]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [15, 16]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [15]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [15, 16]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z [15]	5	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to High Z [15, 16]	–	18	ns
Write Cycle [17]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [15, 16]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [15]	10	–	ns

Notes

13. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 5.
14. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. See application note AN13842 for further clarification.
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
16. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No.1: Address Transition Controlled [18, 19]

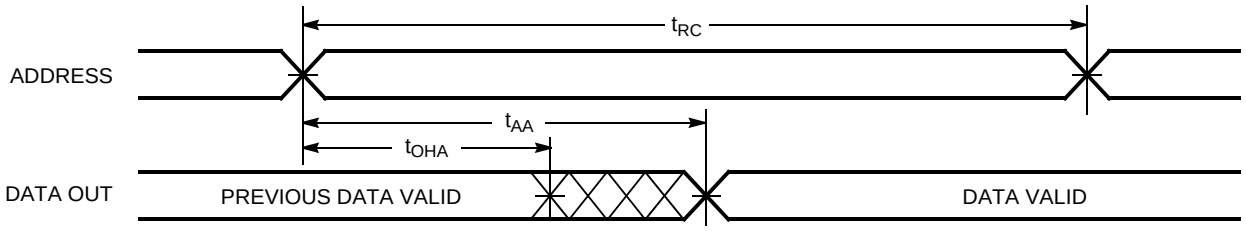
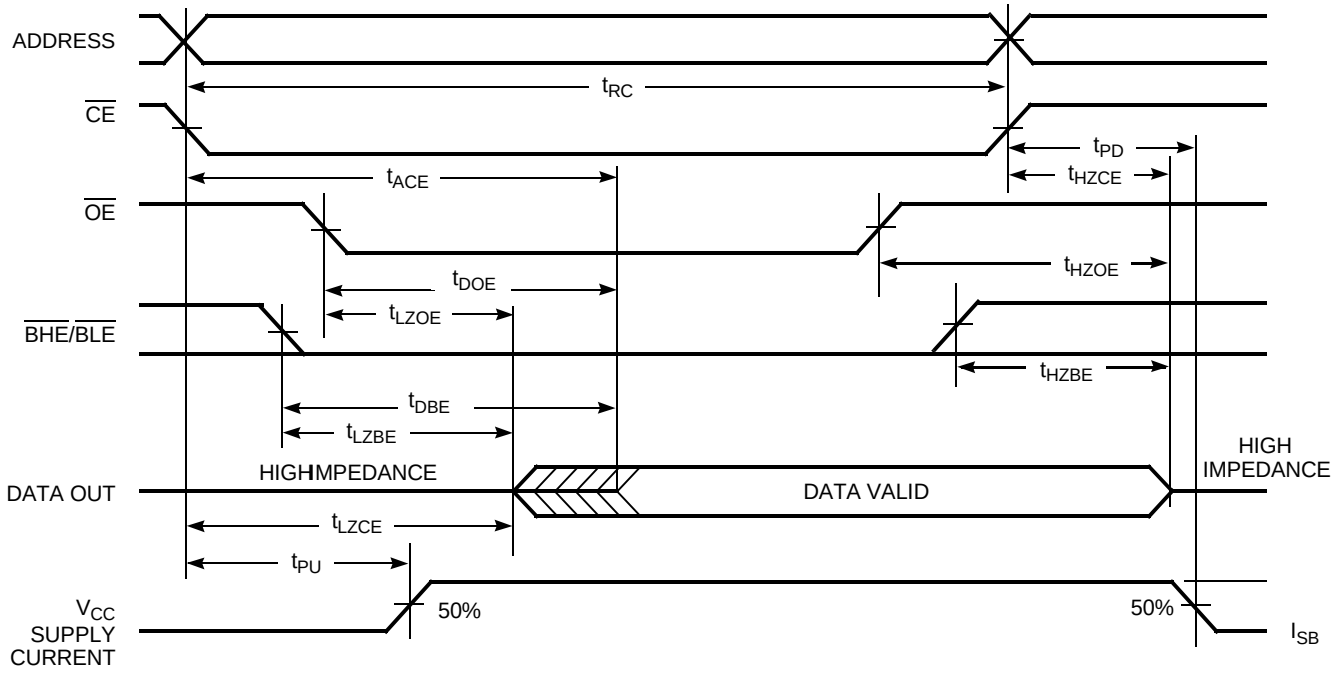


Figure 5. Read Cycle No. 2: $\overline{OE}$ Controlled [19, 20]



Notes
18. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
19. $\overline{WE}$ is HIGH for read cycle.
20. Address valid before or similar to $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle 1: $\overline{WE}$ Controlled [21, 22, 23]

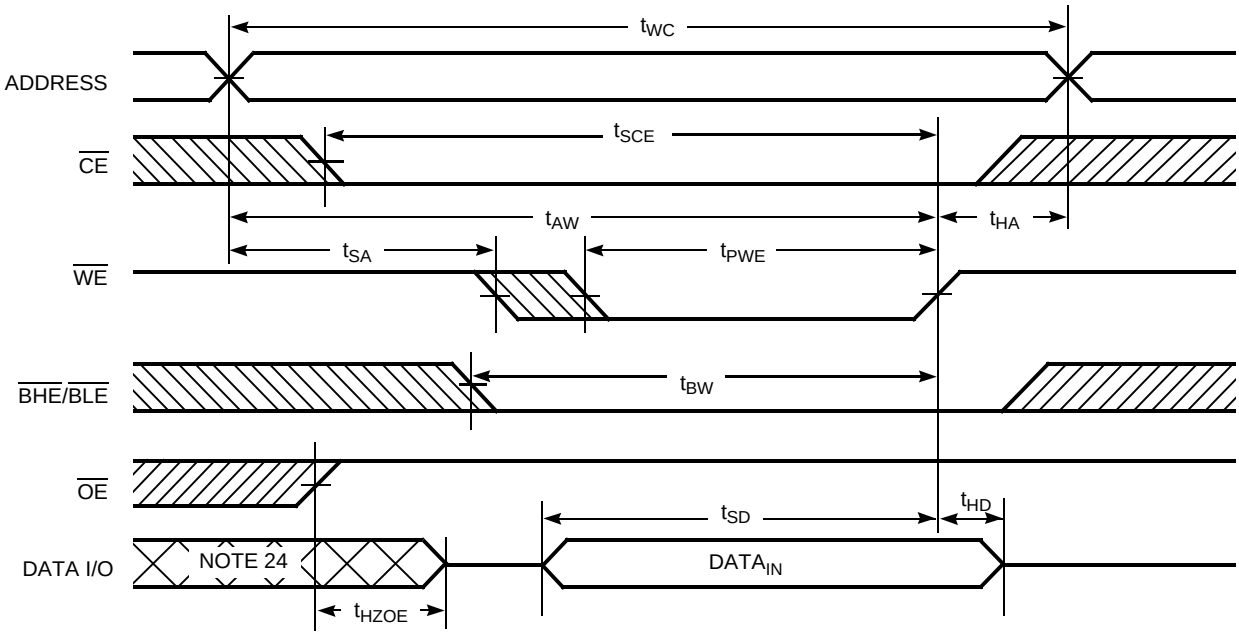
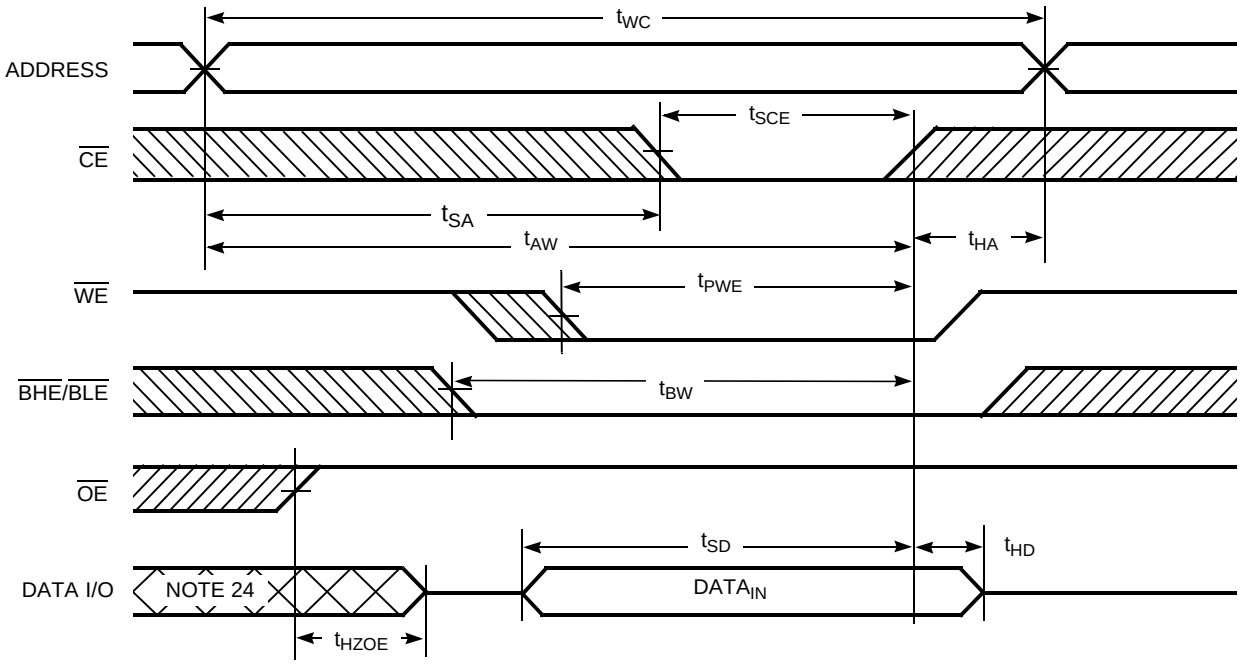


Figure 7. Write Cycle 2: $\overline{CE}$ Controlled [21, 22, 23]



Notes

21. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
22. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
23. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate the write by going inactive. The input setup and hold timing must be referenced to the dge of the signal that terminate the write.
24. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle 3: $\overline{WE}$ controlled, $\overline{OE}$ LOW [25, 26]

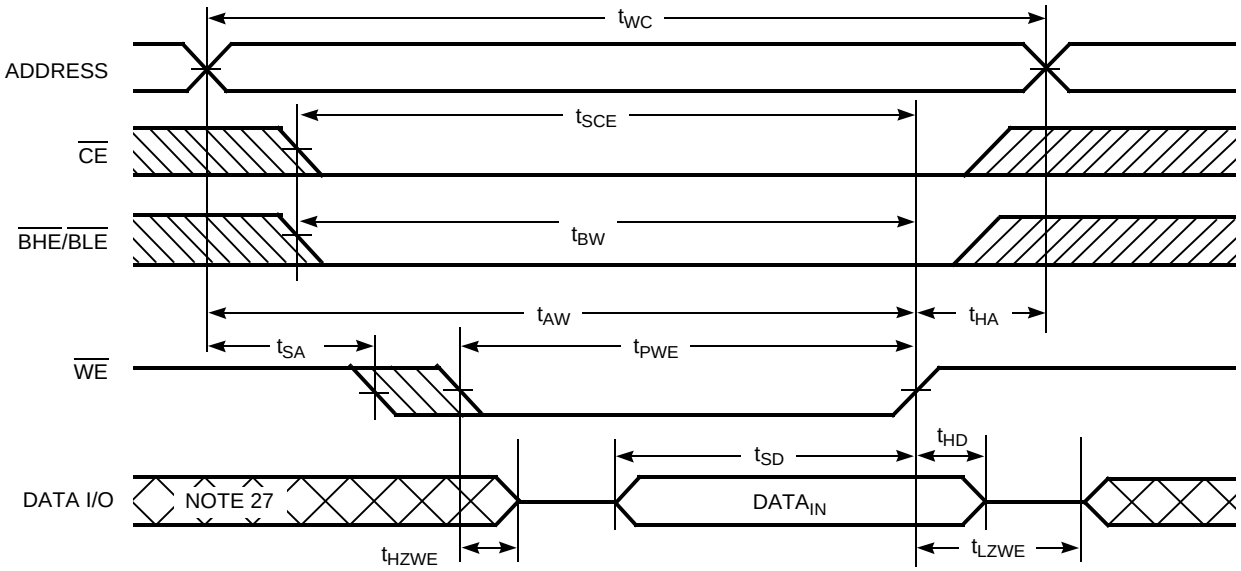
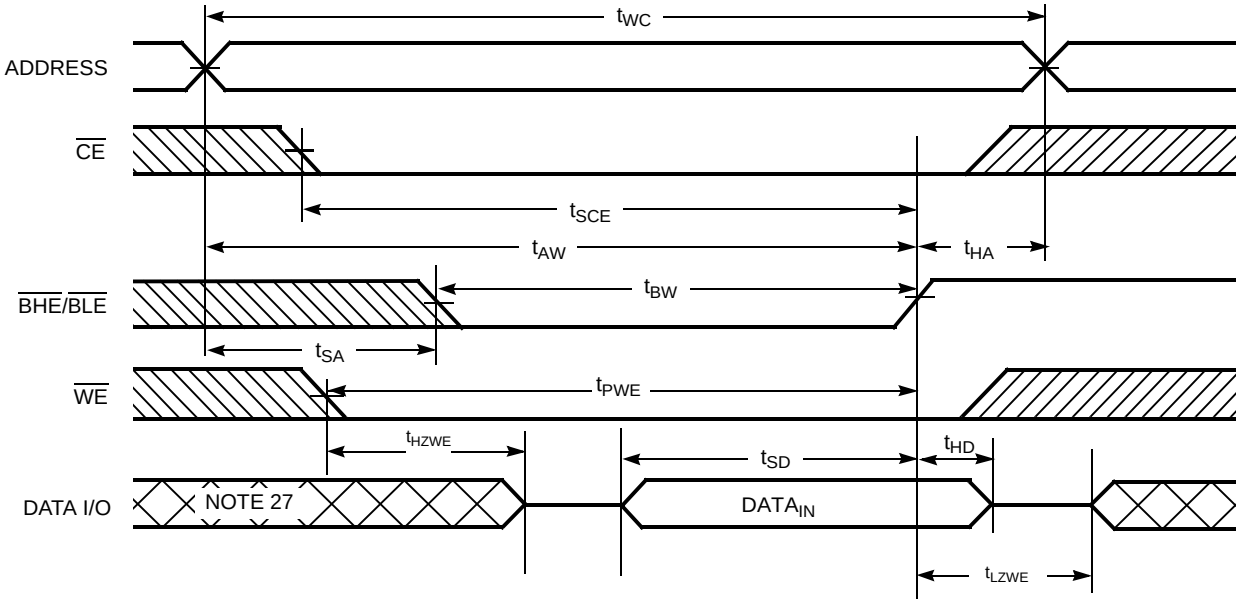


Figure 9. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW [25, 26]



Notes

25. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
26. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate the write by going inactive. The input setup and hold timing must be referenced to the dge of the signal that terminate the write.
27. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$ [28]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X [28]	X [28]	High Z	Deselect/power down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

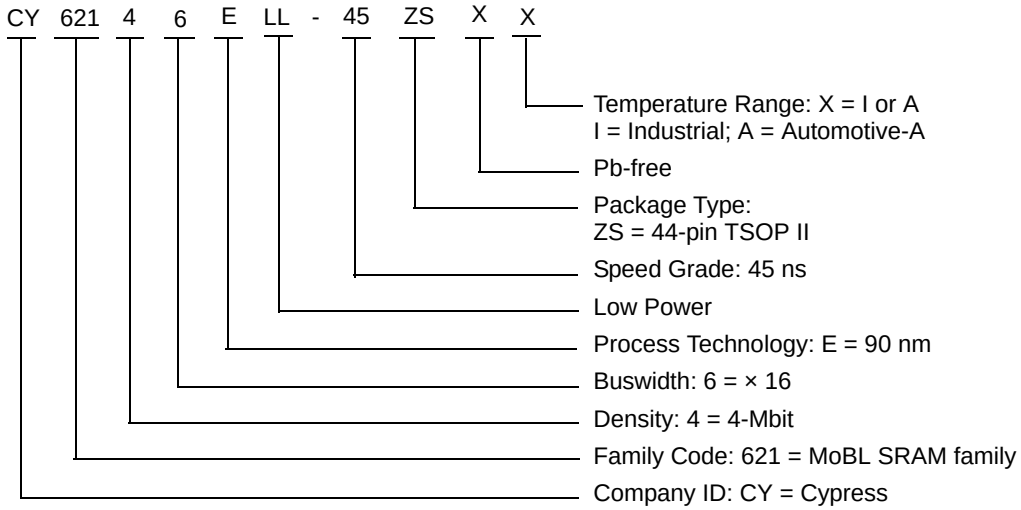
Note
28. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) must be at CMOS levels (not floating) to meet the I_{SB2} / I_{CCDR} spec. Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62146ELL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial
	CY62146ELL-45ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A

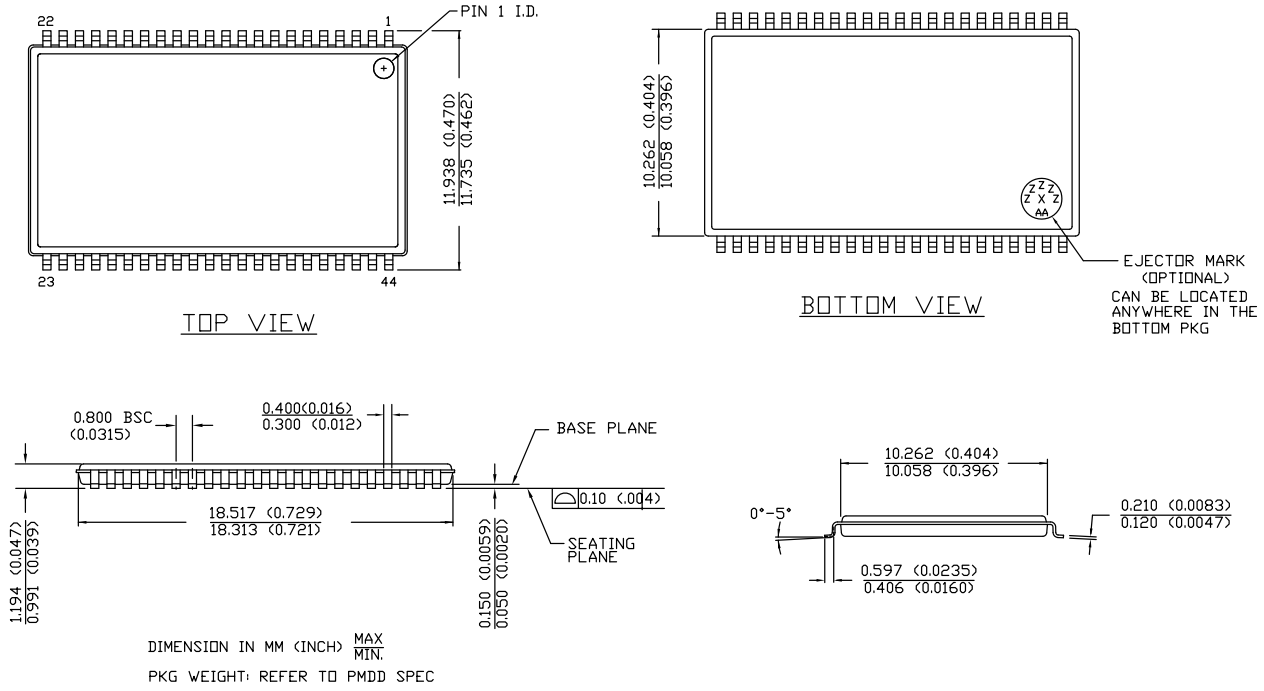
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Gird Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62146E MoBL®, 4-Mbit (256 K × 16) Static RAM Document Number: 001-07970				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	463213	See ECN	NXR	New data sheet.
*A	684343	See ECN	VKN	Added Preliminary Automotive-A Information Updated Ordering Information Table
*B	925501	See ECN	VKN	Added footnote #8 related to I_{SB2} and I_{CCDR} Added footnote #13 related AC timing parameters
*C	1045260	See ECN	VKN	Converted Automotive-A specs from preliminary to final
*D	2073548	See ECN	VKN / AESA	Corrected typo in the Data Retention Waveform and removed its irrelevant footnote
*E	2943752	06/03/2010	VKN	Added Contents Added footnote related to chip enable in Truth Table Updated Package Diagram Added Sales, Solutions, and Legal Information
*F	3109050	12/13/2010	PRAS	Changed Table Footnotes to Footnotes. Added Ordering Code Definitions.
*G	3149059	01/20/2011	RAME	Updated as per latest template Corrected Errors in Ordering Code Definitions Added Acronyms and Units of Measure.
*H	3296704	06/29/11	RAME	Removed reference to AN1064 SRAM system guidelines
*I	3921993	03/05/2013	MEMJ	Updated Switching Waveforms: Added Note 23 and refered the same note in Figure 6, Figure 7. Removed Note “WE is HIGH for read cycle.” and its references in Figure 6, Figure 7. Added Note 26 and refered the same note in Figure 8, Figure 9. Updated Package Diagram: spec 51-85087 – Changed revision from *C to *E.

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